700 to 2700MHz Quadrature Demodulator

Preliminary Technical Data

ADL5382

FEATURES

I/Q Demodulator
Operating RF frequency
700 MHz to 2700MHz
IIP3 +30 dBm
IIP2 +60dBm
Input P1dB +13dBm
NF 14 dB @ 900MHz
Voltage Conversion Gain of 5dB
Quadrature demodulation accuracy
Phase accuracy <0.5°
Amplitude balance <0.25 dB
LO Input –10 to +5 dBm
Demodulation Bandwidth ~500 MHz
I/Q Drive $2V_{pk}$ into 200Ω
Programmable Power Consumption

APPLICATIONS

QAM/QPSK demodulator
W-CDMA/CDMA/CDMA2000/GSM
Point-to-(Multi)Point Radio
WiMax

FUNCTIONAL BLOCK DIAGRAM

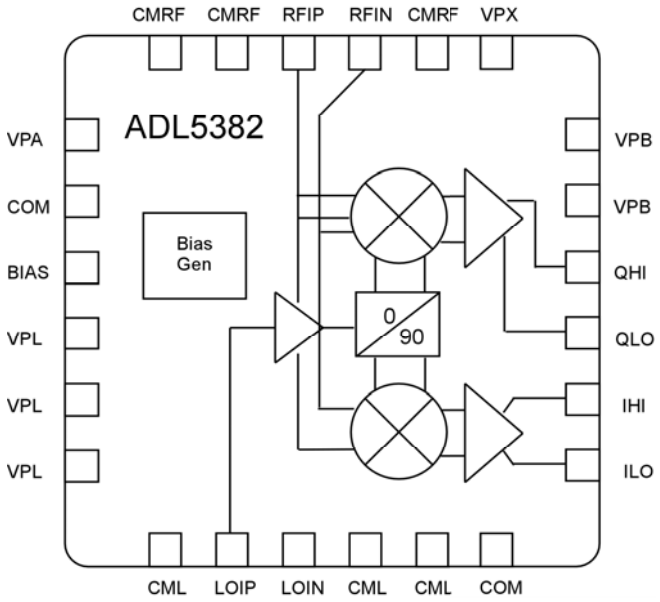

Figure 1.

GENERAL DESCRIPTION

The ADL5382 is a high performance quadrature I-Q demodulator that covers an RF input frequency range from 700 MHz to 2.7 GHz. With a NF = 14dB, IP1dB = 13dBm and IIP3 = 30dBm, the demodulator offers outstanding dynamic range suitable for the demanding infrastructure direct-conversion requirements. The differential RF inputs provide a well-behaved broad-band input impedance of 50Ω and should be driven from a 1:1 balun for best performance.

Excellent quadrature accuracy is achieved using on-chip poly-phase filters for LO quadrature generation. Over a wide range of local oscillator (LO) levels, excellent demodulation accuracy is achieved with phase and amplitude balances < 0.25 dB and < 0.5°, respectively. The demodulated in-phase (I) and quadrature (Q) differential outputs are fully buffered. The ADL5382 provides voltage conversion gain of 5dB independent of differential load impedances that can be as low as 100 Ω with a drive capability exceeding $2V_{pp}$ in to 200 Ω.

The fully balanced design minimizes effects from 2nd order distortion. The leakage from the LO port to the RF port is <-60dBc. Differential DC-offsets at the I and Q outputs are <10mV. Both of these factors contribute to the excellent IIP2 of >60dBm.

The ADL5382 operates off a 4.75V to 5.25V supply. The supply current is programmable with an external resistor from the BIAS pin to ground. The ADL5382 is fabricated using Analog Devices' advanced Silicon-Germanium bipolar process and is available in a 24-lead exposed paddle LFCSP package. Performance is specified over a -40°C to +85°C temperature range.

Rev. PrC

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REVISION HISTORY

11/07—Rev. B to Rev. C

SPECIFICATIONS

Table 1. V_S = 5 V, T_A = 25°C, F_{LO} = 1960 MHz, F_{IF} = 10 MHz, P_{LO} = 0 dBm, BIAS pin open, Zo= 50 Ω unless otherwise noted. I & Q are loaded to 50 Ω using a 9:1 balun.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range		0.7		2.7	GHz
RF Frequency Range		0.7		2.7	GHz
RF INPUT @ 900MHz	RFIP, RFIN				
Input Impedance	Differential		50		Ω
Input P1dB			13		dBm
Second Order Input Intercept (IIP2)	+3 dBm Each Tone		65		dBm
Third Order Input Intercept (IIP3)	0 dBm Each Tone		30		dBm
Noise Figure					
			14		dB
	With a -4dBm interferer 5MHz away		20		dB
RF INPUT @ 1950MHz					
Input Impedance	Differential		50		Ω
Input P1dB			13		dBm
Second Order Input Intercept (IIP2)	+3 dBm Each Tone		58		dBm
Third Order Input Intercept (IIP3)	0 dBm Each Tone		28		dBm
Noise Figure					
			16		dB
	With a -4dBm interferer 5MHz away		TBD		dB
LO INPUT	LOIP, LOIN				
Input Return Loss	AC-coupled into LOIP with LOIN bypassed, measured at 2GHz		9		dB
LO input level		-10		5	dBm
LO-RF Leakage	RFIN,RFIP terminated in 50 Ω		–60		dBc
I/Q BASEBAND OUTPUTS	QHI, QLO, IHI, ILO				
Voltage Conversion Gain	450Ω load on QHI, QLO, IHI, ILO		5		dB
	200Ω load		4.5		dB
Demodulation Bandwidth	Small Signal 3 dB Bandwidth		500		MHz
	1Vp-p Signal 3 dB Bandwidth		TBD		MHz
Quadrature Phase Error	700 Mhz to 2700 Mhz		0.5		deg
			0.1		dB
I/Q Amplitude Imbalance					
Output DC Offset (Differential)			10		mV
	0dBm LO input				
Output Common-Mode			Vpos-3		V
Group Delay Flatness	Any 20 MHz		TBD		ns p-p
Gain Flatness	Any 20 MHz		TBD		dB p-p
Output Swing	Differential 200 Ω load		2		Vp-p
	1kΩ load		TBD		Vp-p
Peak Output Current	Each pin		10		mA
POWER SUPPLIES	VPA,VPL,VPB,VPX				
Voltage		4.75		5.25	V
Current	BIAS pin open		220		mA
	RBIAS=4kΩ		195		mA

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Supply Voltage VPOS1, VPOS2, VPOS3	5.5 V
LO Input Power	10 dBm (re: 50 Ω)
RF/IF Input Power	TBD dBm (re: 50 Ω)
Internal Max Power Dissipation	TBD mW
θ_{JA}	TBD°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

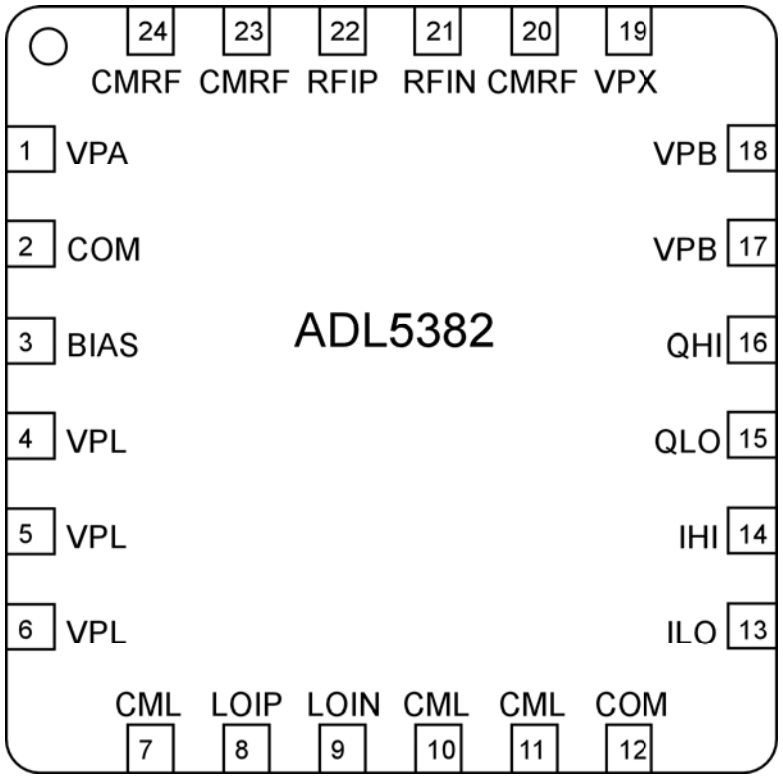

Figure 2. 24-Lead LFCSP

Table 2. Pin Function Descriptions—28-Lead TSSOP

Pin No.	Mnemonic	Description
1, 4, 5,6, 17, 18, 19	VPA, VPL, VPB, VPX	**Supply**: Positive Supply for LO, IF, and Biasing and Baseband Sections, respectively. These pins should be decoupled to board ground using appropriate sized capacitors.
2, 7, 10, 11,12, 20, 23, 24	COM, CML, CMRF	**Ground**: Connect to a low impedance ground plane.
3	BIAS	**Bias Control**: A resistor can be connected between BIAS and COM to adjust the bias to the mixer core. The default setting for this pin is open.
8, 9	LOIP, LOIN	**Local Oscillator**: A single-ended LO at 0 dBm can be applied through a 1000 pF capacitor to LOIP. LOIN should be ac-grounded, also using a 1000 pF. These inputs can also be driven differentially through a balun (recommended balun is M/A-COM ETC1-1-13).
13, 14, 15, 16	ILO, IHI, QLO, QHI	**I-Channel and Q-Channel Mixer Baseband Outputs**: These are low impedance outputs. The bias level on these pins is equal to VPOS-3V. Each output pair can swing 2 Vpp (differential) into a load of 200 ohms. Output 3 dB bandwidth is 240 MHz
21, 22	RFIN, RFIP	**RF Input**: A single-ended 50 Ω signal can be applied to the RF inputs through a 1:1 Balun (recommended balun is M/A-COM ETC1-1-13; Use Johanson Technology balun for high frequency operation). Ground-referenced inductors must also be connected to RFIP and RFIN (recommended values = 34 nH).
	EP	**Exposed Paddle**: Connect to a low impedance ground plane

TYPICAL PERFORMANCE CHARACTERISTICS

V_S=5V, T=25°C, System Impedance Zo = 50Ω , Bias Resistor open unless otherwise noted

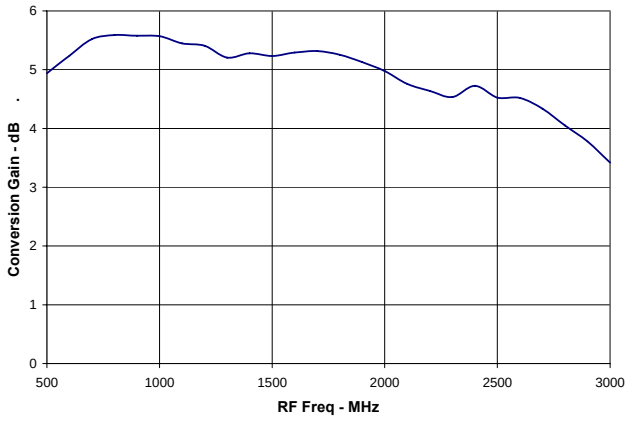

Figure 3. Gain vs. Frequency

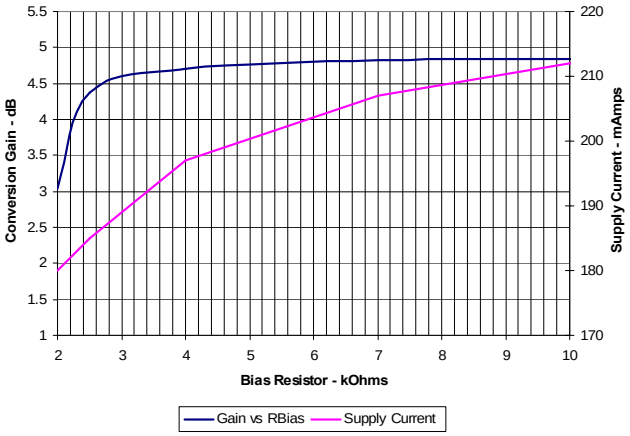

Figure 6. Conversion Gain and Supply Current vs. Bias Resistor at 1950MHz

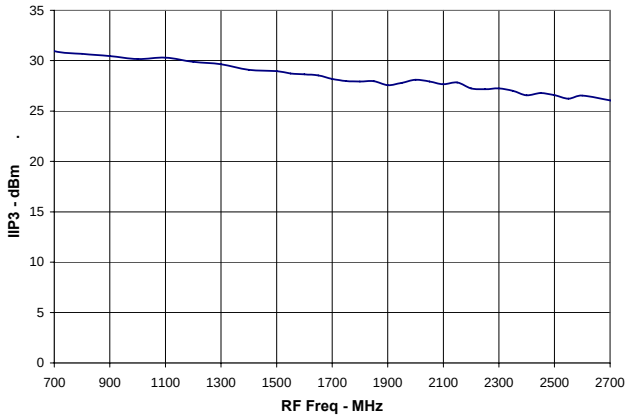

Figure 4.IIP3 vs. Frequency

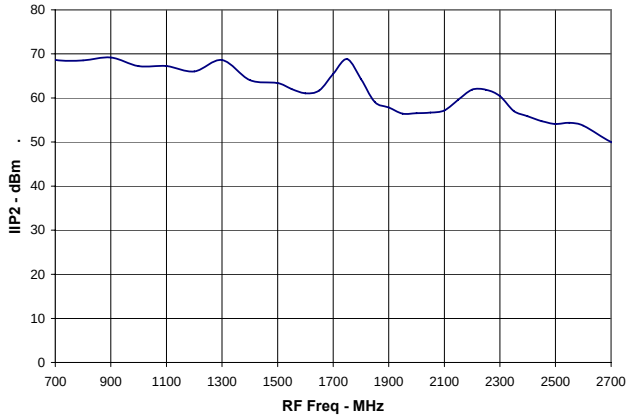

Figure 7. IIP2 vs. Frequency

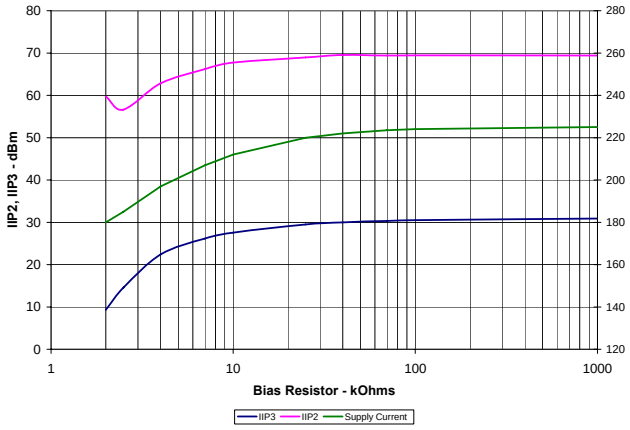

Figure 5. IIP3, IIP2 and Supply Current vs. Bias Resistor at 900 MHz

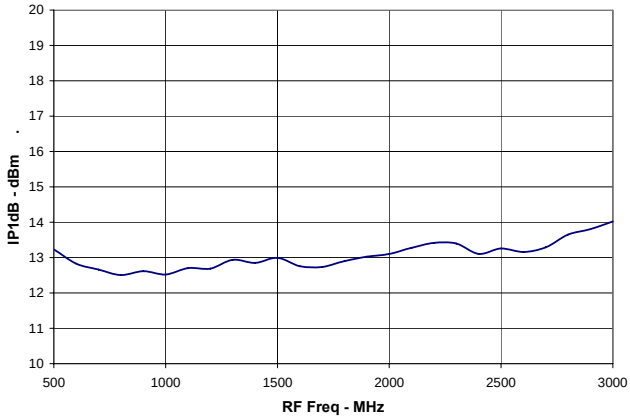

Figure 8. IP1dB vs. Frequency

V_S=5V, T=25°C, System Impedance Zo = 50Ω , Bias Resistor open unless otherwise noted

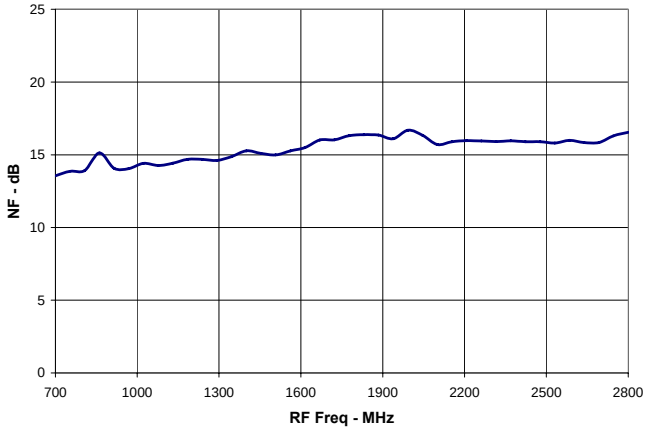

Figure 9. Noise Figure vs. Frequency

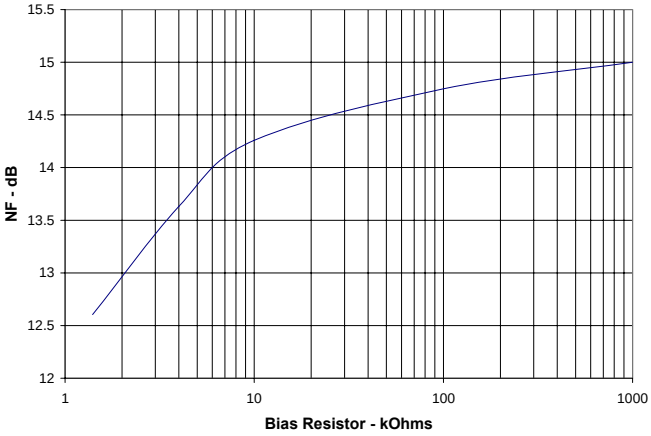

Figure 12. Noise Figure vs. Bias Resistor at 900MHz

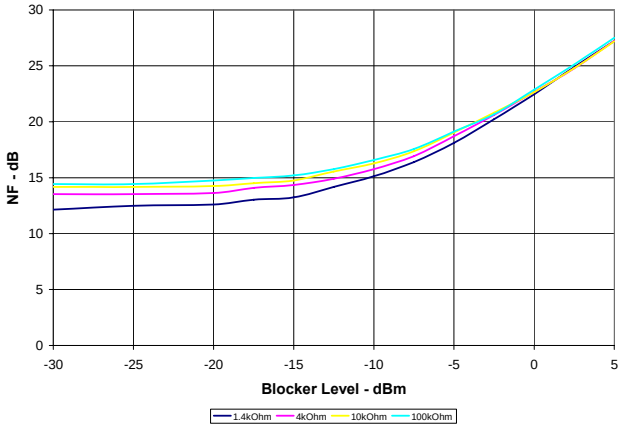

Figure 10. NF Under Blocking at 900MHz for several Bias Resistor Values (Blocker offset by 5MHz)

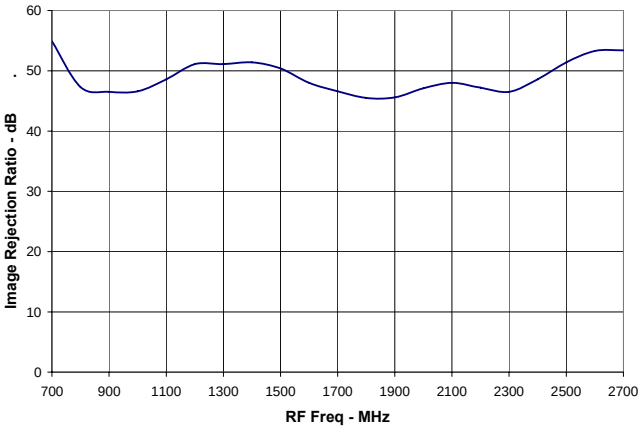

Figure 13. Image Rejection for 5MHz Low-IF WCDMA waveform

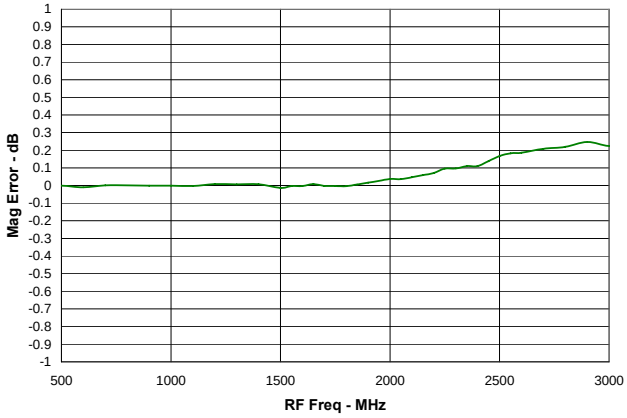

Figure 11. IQ Quadrature Magnitude Imbalance

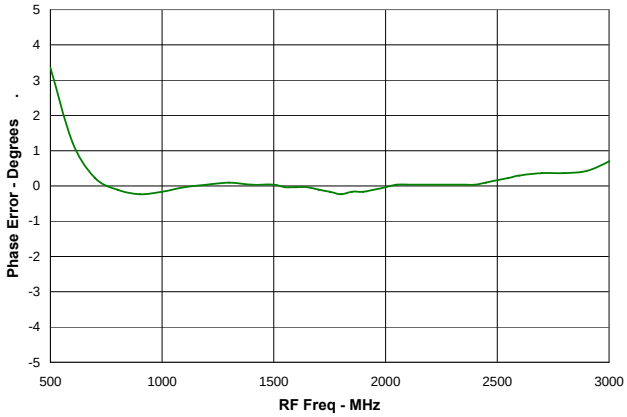

Figure 14. IQ Quadrature Phase Imbalance

CIRCUIT DESCRIPTION

The ADL5382 can be divided into five sections: the local oscillator (LO) interface, the RF voltage-to-current (V-to-I) converter, the mixers, the differential Emitter follower outputs, and the bias circuit. A detailed block diagram of the device is shown in Figure 15.

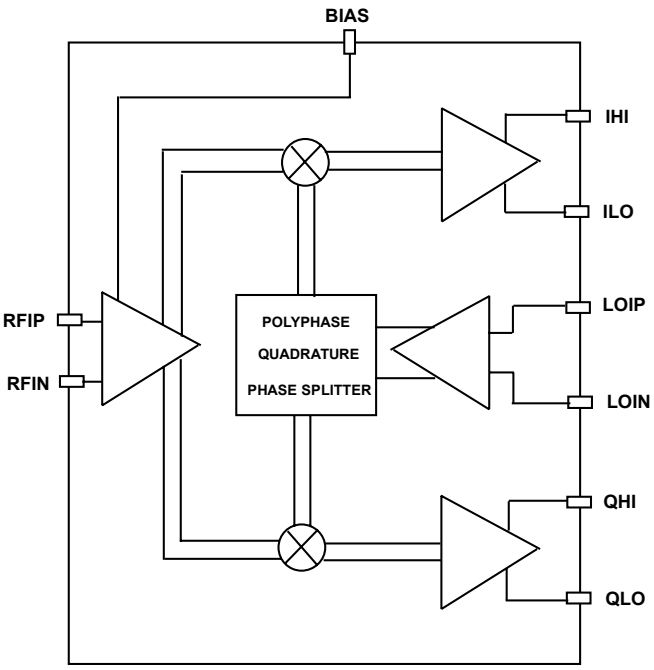

Figure 15. ADL5382 Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. RF signals are converted into currents by the V-to-I converters that feed into the two mixers. The differential I and Q outputs of the mixers are buffered via emitter followers. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a buffer amplifier followed by a poly-phase filter which provides quadrature related output signals. Each signal is then amplified and amplitude-limited to drive the double-balanced mixers.

V-TO-I CONVERTER

The differential RF input signal is applied to a resistively degenerated common base stage, which converts the differential input voltage to output currents. The output currents then mix with the quadrature related LO signals in the mixer stage.

MIXERS

The ADL5387 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads which then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off chip. The output impedance is set by on chip 25 ohm series resistors which yields a 50 ohm differential output impedance for each Baseband port. The fixed output impedance will form a voltage divider with the load impedance which will reduce the effective gain. For example a 500 ohm differential load will have 1dB lower effective gain than a high (10Kohm) differential load impedance.

BIAS CIRCUIT

A band gap reference circuit generates the proportional-to-absolute-temperature (PTAT) as well as temperature-independent reference currents used by different sections. The mixer current can be reduced via an external resistor between the BIAS pin and ground. When the BIAS pin is open the mixer runs at maximum current and hence the greatest dynamic range. The mixer current can be reduced by placing a resistance to ground, hence reducing over all power consumption, noise figure and IIP3. The effect on each of these parameters is shown in figure 5, figure 6, and figure 12

EVALUATION BOARD

The ADL5382 evaluation board is available. The board can be used for single-ended or differential baseband analysis. The default configuration of the board is for single-ended baseband analysis.

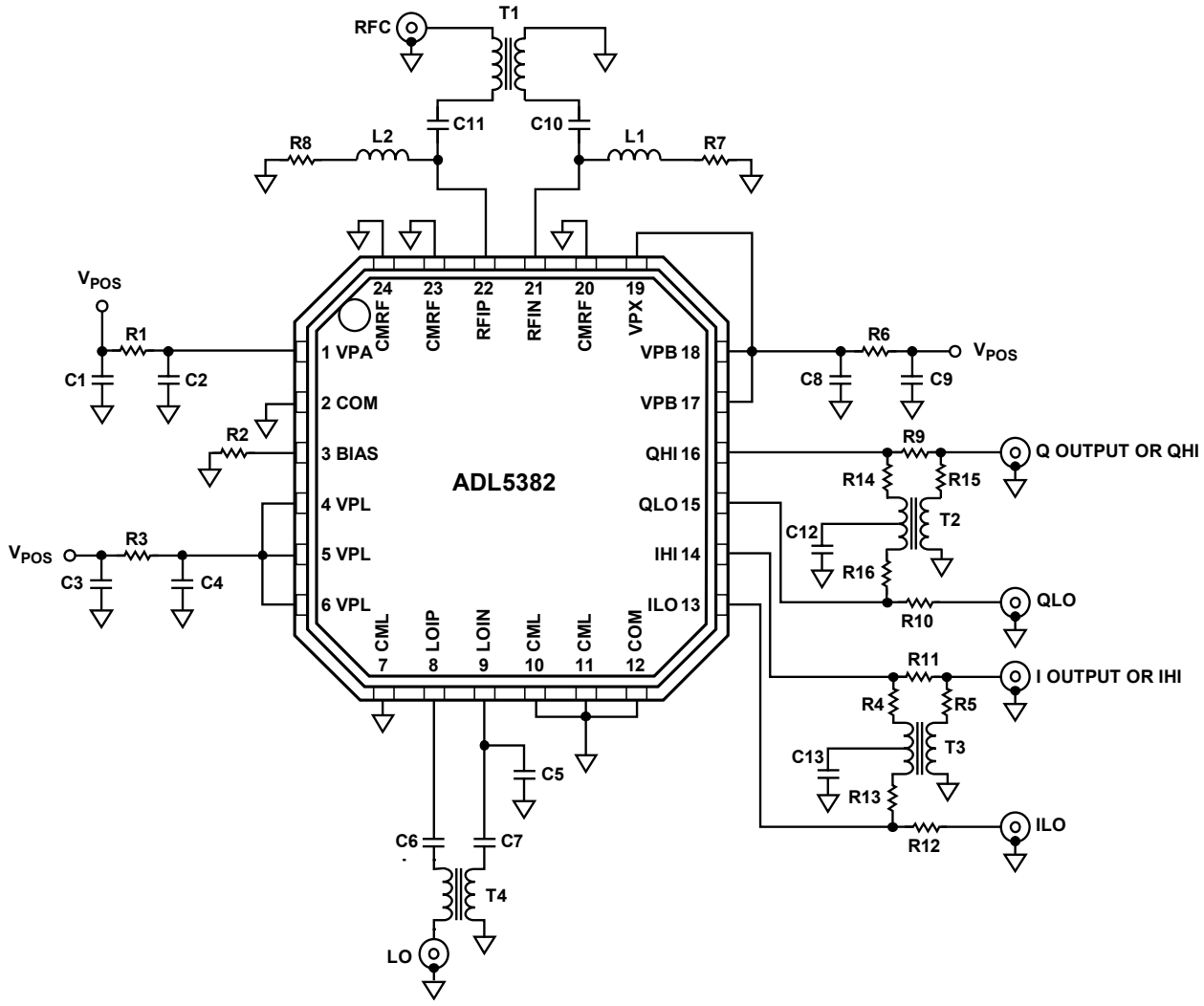

Figure 16. Evaluation Board Schematic

Table 3. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Vector Pins.	Not Applicable
R1, R3, R6	Power Supply Decoupling. Shorts or power supply decoupling resistors.	R1, R3, R6 = 0 Ω (0603)
C1, C2, C3, C4, C8, C9	The capacitors provide the required dc coupling up to 2 GHz.	C2, C4, C8 = 100 pF (0402) C1, C3, C9 = 0.1 µF (0603)
C5, C6, C7, C10, C11	AC Coupling Capacitors. These capacitors provide the required ac coupling from 700MHz to 2.7GHz.	C5, C6, C10, C11 = 1000 pF (0402), C7 = Open
R4, R5, R9 to R16	Single-Ended Baseband Output Path. This is the default configuration of the evaluation board. R14 to R16 and R4, R5, and R13 are populated for appropriate balun interface. R9, R10 and R11, R12 are not populated. Baseband outputs are taken from QHI and IHI. The user can reconfigure the board to use full differential baseband outputs. R9 to R12 provide a means to bypass the 9:1 TCM9-1 transformer to allow for differential baseband outputs. Access the differential baseband signals by populating R9 to R12 with 0 Ω and not populating R4, R5, R13 to R16. This way the transformer does not need to be removed. The baseband outputs are taken from the SMAs of Q_HI, Q_LO, I_HI, and I_LO.	R4, R5, R13 to R16 = 0 Ω (0402), R9 to R12 = Open
L1, L2, R7, R8	Input Biasing. Inductance and resistance sets the input biasing of the common base input stage. Default value is 33 nH.	L1, L2 = 33 nH (0603CS-Coilcraft), R7, R8 = 0 Ω (0402)
T2, T3	IF Output Interface. TCM9-1 converts a differential high impedance IF output to a single-ended output. When loaded with 50 Ω, this balun presents a 450 Ω load to the device. The center tap can be decoupled through a capacitor to ground.	T2, T3 = TCM9-1, 9:1 (Mini-Circuits)
C12, C13	Decoupling Capacitors. C12 and C13 are the decoupling capacitors used to reject noise on the center tap of the TCM9-1.	C12, C13 = 0.1 µF (0402)
T4	LO Input Interface. The LO is driven as a differentially. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T4 = ETC1-1-13, 1:1 (M/A COM)
T1	RF Input Interface. ETC1-1-13 is a 1:1 RF balun that converts the single-ended RF input to differential signal.	T1 = ETC1-1-13, 1:1 (M/A COM)
R2	R_{BIAS}. Optional bias setting resistor. See the Circuit Description section to see how to use this feature.	R2 = Open

OUTLINE DIMENSIONS

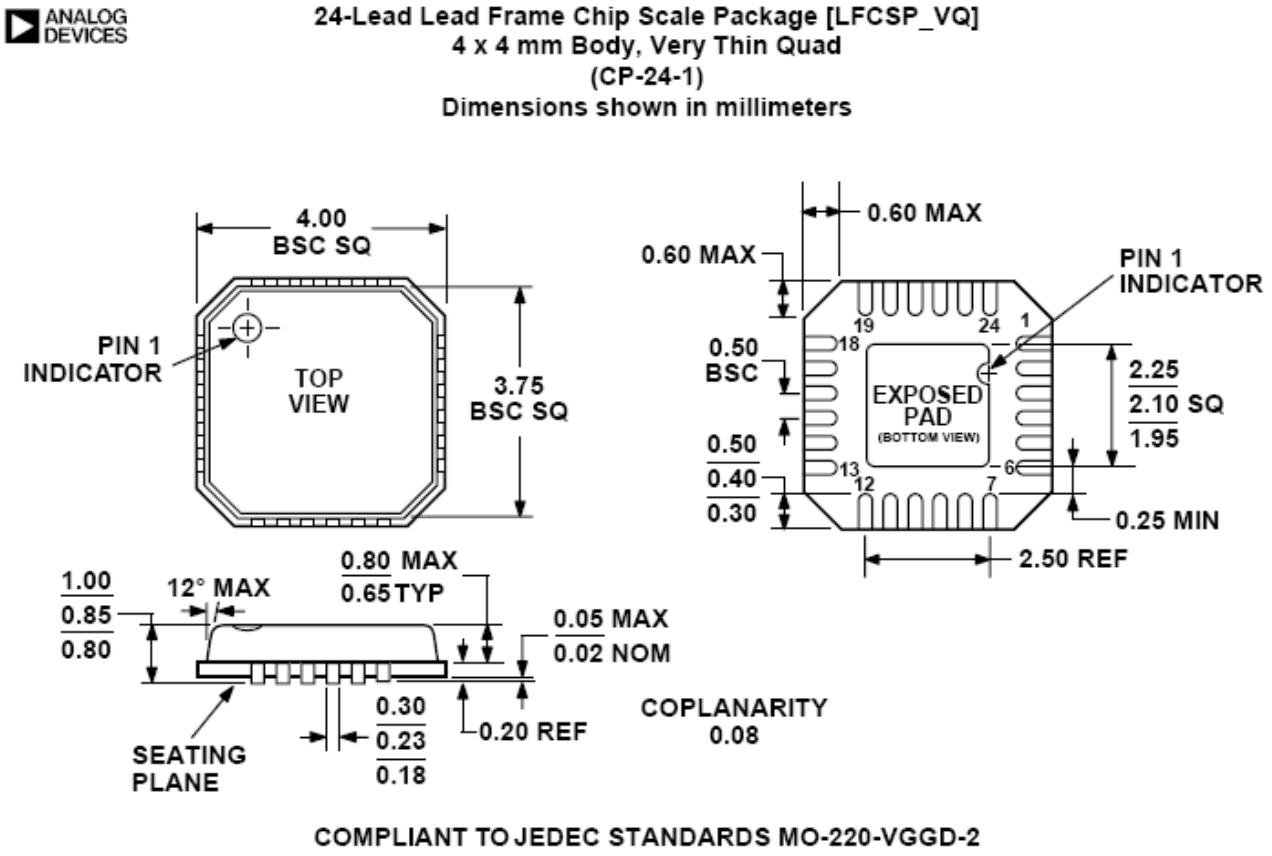

Figure 17. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ] 4 mm × 4 mm Body, Very Thin Quad (CP-24-2)

Dimensions shown in millimeters

ESD CAUTION

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADL5382ACPZ-R7	–40°C to +85°C	7″ Tape and Reel	
ADL5382ACPZ-WP	–40°C to +85°C	Waffle Pack	
ADL5382-EVALZ		Evaluation Board	